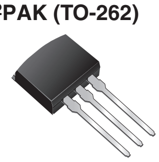
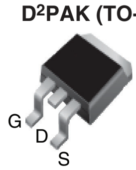
Power MOSFET

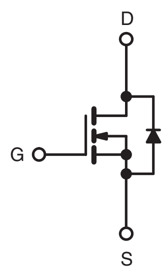
PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.018
Q_g (Max.) (nC)	110	
Q_{gs} (nC)	29	
Q_{gd} (nC)	36	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- Advanced Process Technology
- Surface Mount (IRFZ48S/SiHFZ48S)
- Low-Profile Through-Hole (IRFZ48L/SiHFZ48L)
- 175 °C Operating Temperature
- Fast Switching
- Lead (Pb)-free Available

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface mount application.

The through-hole version (IRFZ48L/SiHFZ48L) is available for low-profile applications.

ORDERING INFORMATION			
Package	D²PAK (TO-263)	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free	IRFZ48SPbF	-	IRFZ48LPbF
	SiHFZ48S-E3	-	SiHFZ48L-E3
SnPb	IRFZ48S	IRFZ48STRL	-
	SiHFZ48S	SiHFZ48STL	-

Note
a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current[f]	V_{GS} at 10 V	T_C = 25 °C	I_D	50	A
		T_C = 100 °C		50	
Pulsed Drain Current[a, e]			I_{DM}	290	
Linear Derating Factor				1.3	W/°C
Single Pulse Avalanche Energy[b, e]			E_{AS}	100	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	190	W
	T_A = 25 °C			3.7	
Peak Diode Recovery dV/dt[c, e]			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)[d]	for 10 s			300	

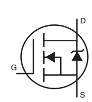
Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, Starting T_J = 25 °C, L = 22 µH, R_G = 25 Ω, I_{AS} = 72 A (see fig. 12).
c. $I_{SD} \le 72$ A, dI/dt ≤ 200 A/µs, $V_{DD} \le V_{DS}$, $T_J \le 175$ °C.
d. 1.6 mm from case.
e. Uses IRFZ48/SiHFZ48 data and test conditions.
f. Calculated continuous current based on maximum allowable junction temperature.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB Mount)[a]	R_{thJA}	-	40	°C / W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA[c]		-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 43 A[b]	-	-	0.018	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V, I_D = 43 A[b]		27	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5[c]		-	2400	-	pF
Output Capacitance	C_{oss}			-	1300	-	
Reverse Transfer Capacitance	C_{rss}			-	190	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 72 A, V_{DS} = 48 V, see fig. 6 and 13[b, c]	-	-	110	nC
Gate-Source Charge	Q_{gs}			-	-	29	
Gate-Drain Charge	Q_{gd}			-	-	36	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 72 A, R_G = 9.1 Ω, R_D = 0.34 Ω, see fig. 10[b, c]		-	8.1	-	ns
Rise Time	t_r			-	250	-	
Turn-Off Delay Time	$t_{d(off)}$			-	210	-	
Fall Time	t_f			-	250	-	
Internal Source Inductance	L_S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	50[c]	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	290	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 72 A, V_{GS} = 0 V[b]		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 72 A, dI/dt = 100 A/µs[b, c]		-	120	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	500	800	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.
c. Uses IRFZ48/SiHFZ48 data and test conditions.
d. Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

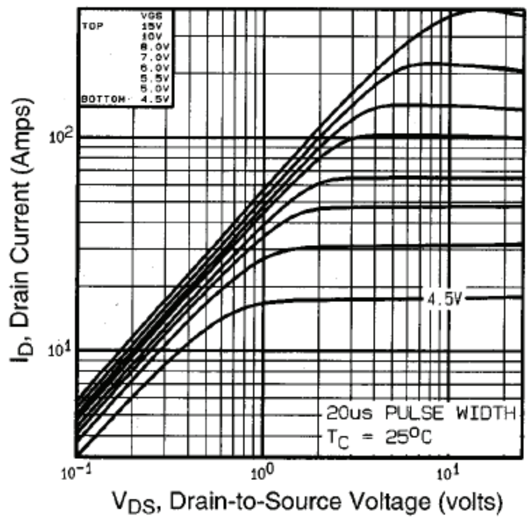


Fig. 1 - Typical Output Characteristics

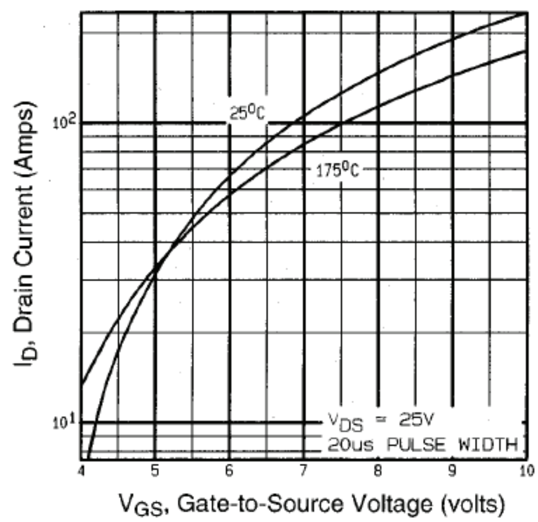


Fig. 3 - Typical Transfer Characteristics

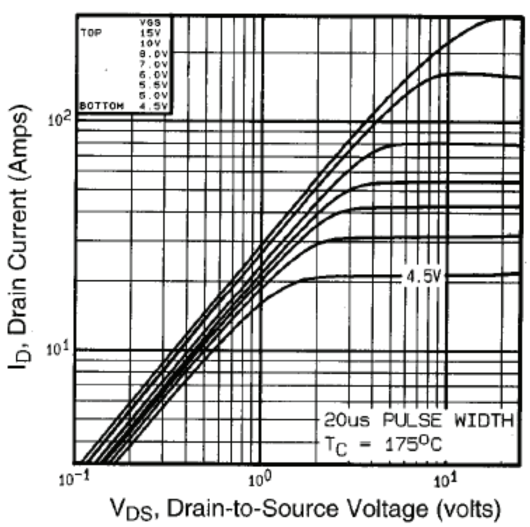


Fig. 2 - Typical Output Characteristics

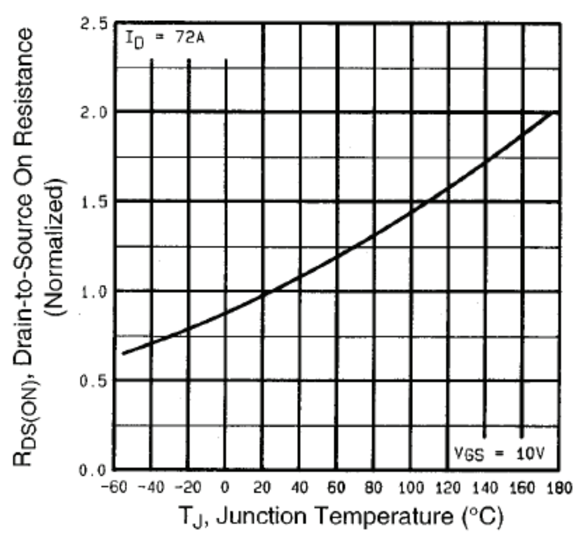


Fig. 4 - Normalized On-Resistance vs. Temperature

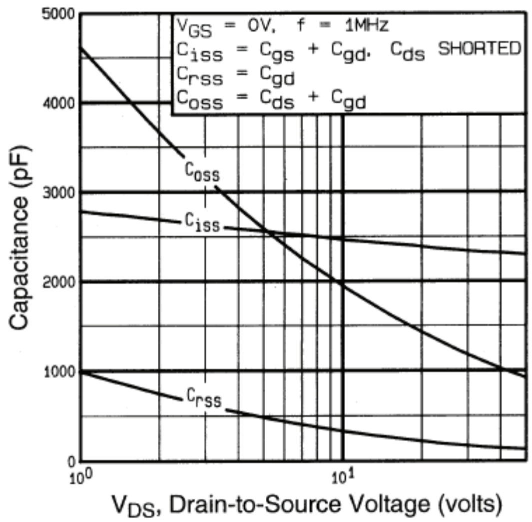


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

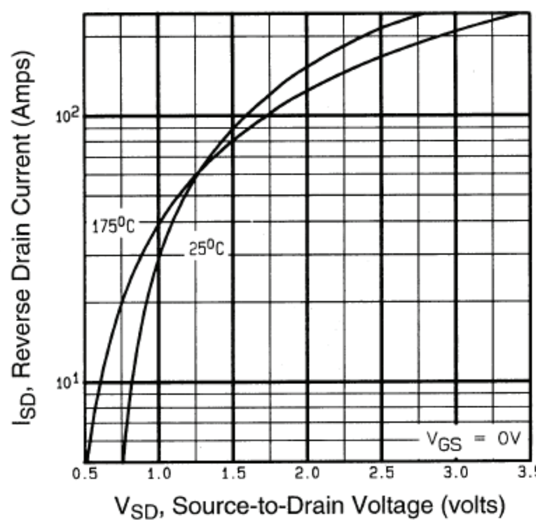


Fig. 7 - Typical Source-Drain Diode Forward Voltage

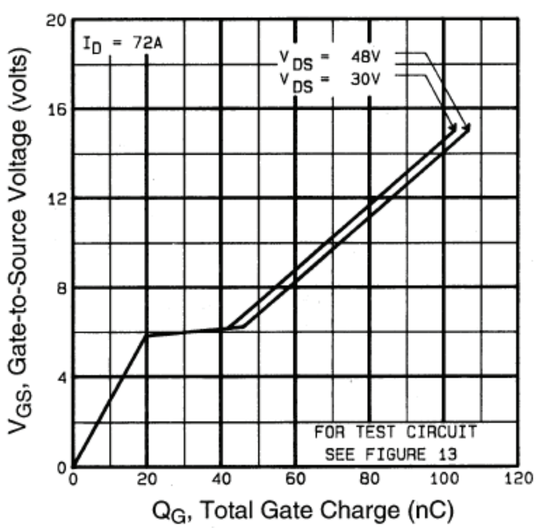


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

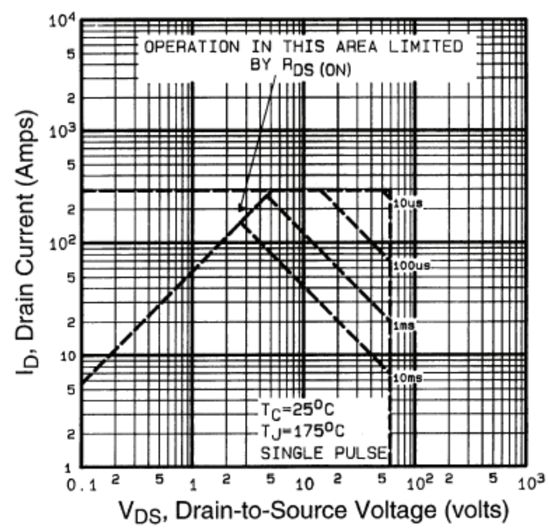


Fig. 8 - Maximum Safe Operating Area

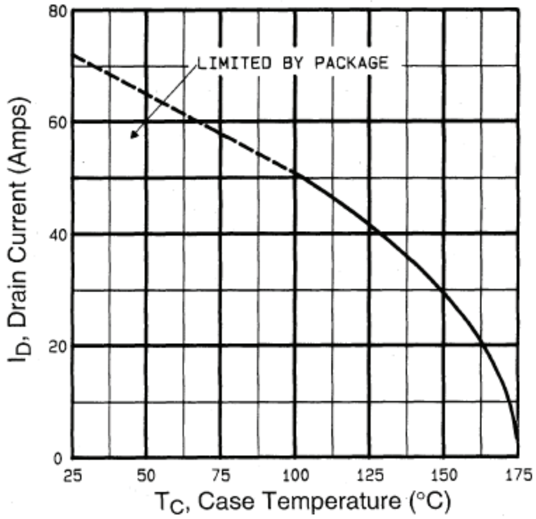


Fig. 9 - Maximum Drain Current vs. Case Temperature

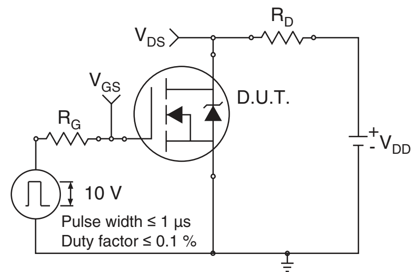


Fig. 10a - Switching Time Test Circuit

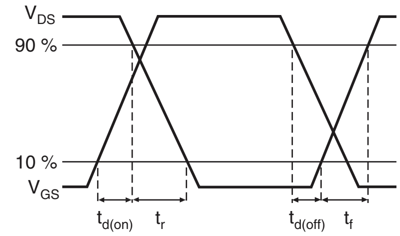


Fig. 10b - Switching Time Waveforms

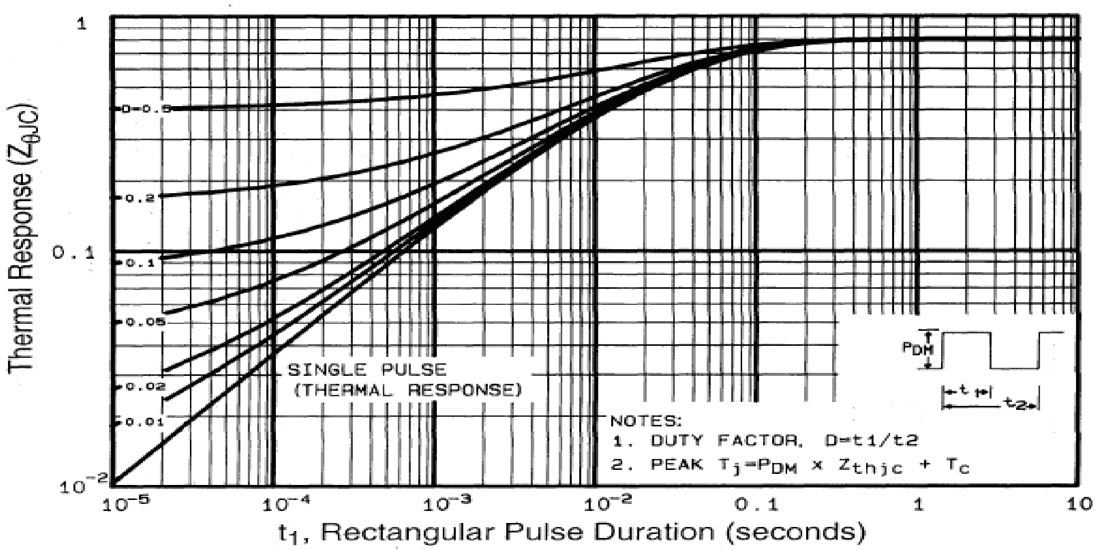


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

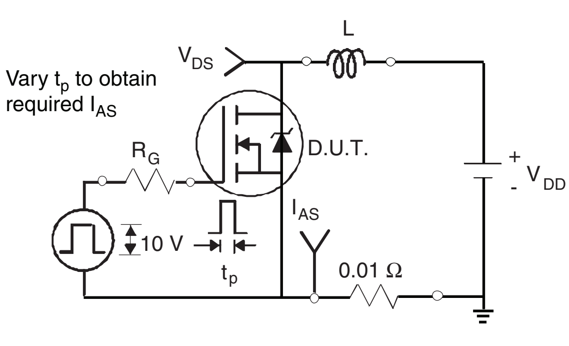


Fig. 12a - Unclamped Inductive Test Circuit

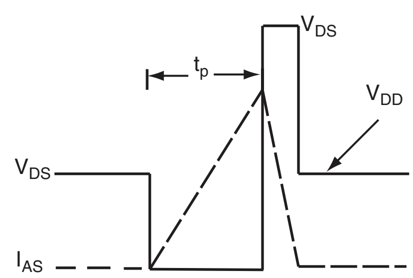


Fig. 12b - Unclamped Inductive Waveforms

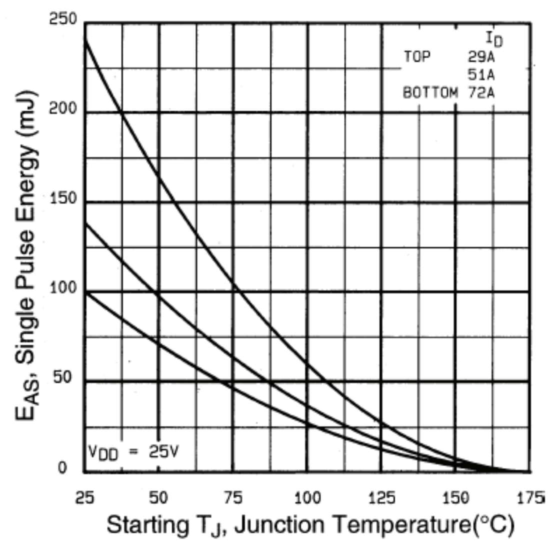


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

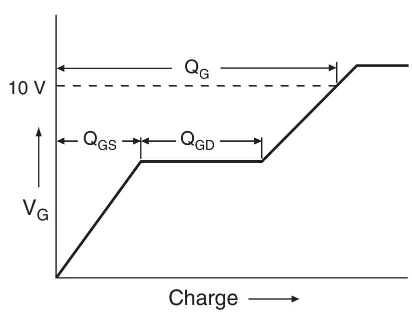


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

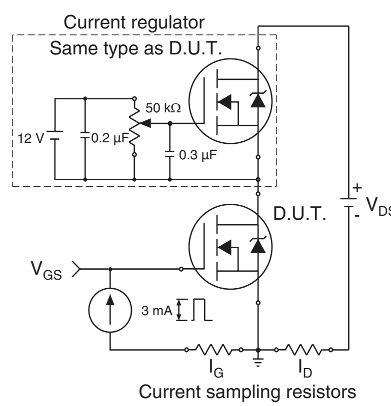


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

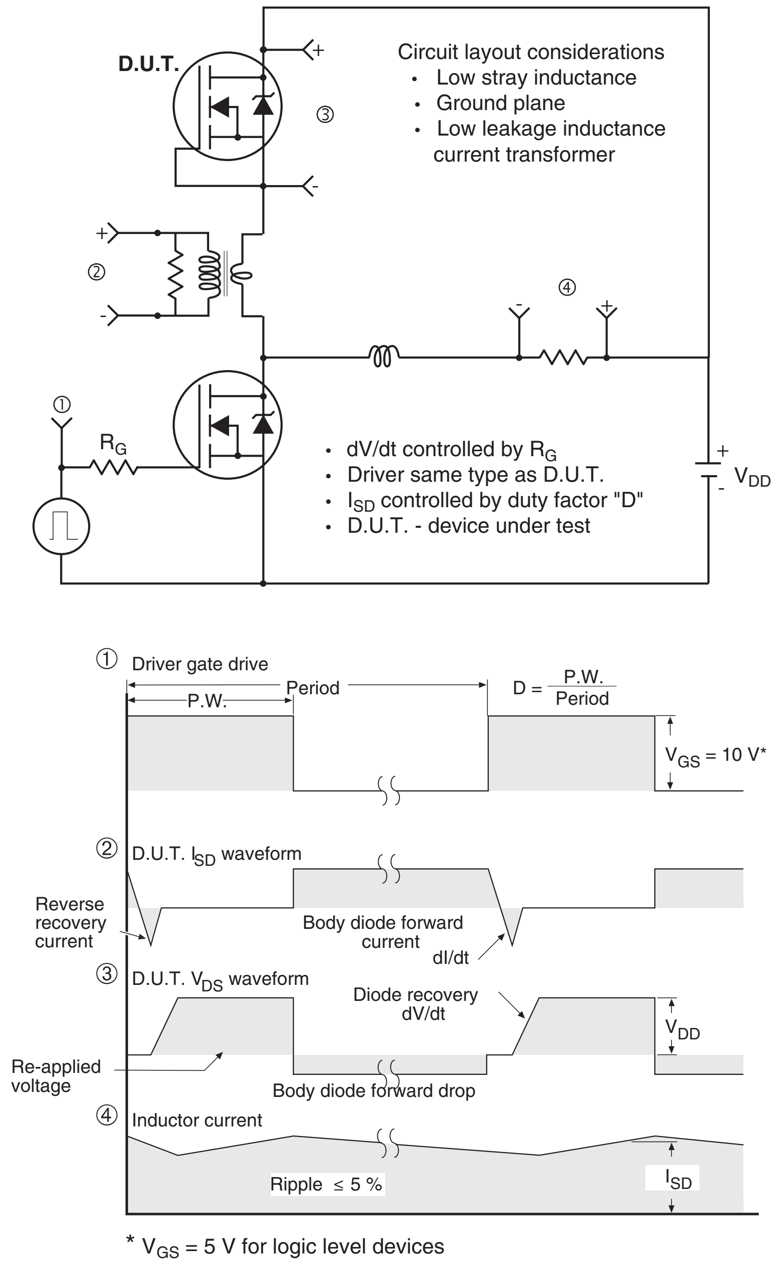


Fig. 14 - For N-Channel

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